CLAIM AMENDMENT

Please **CANCEL** claims 1-3, 5-6, 15-17 and 19.

Please **AMEND** claims 4, 14 and 18, as follows.

1-3. (Cancelled)

4. (Currently Amended) ~~The~~ A liquid crystal display, ~~of claim 3, further~~ comprising:

a first insulating substrate;

a black matrix formed on said first substrate, said black matrix being mesh-shaped with opening portions at pixel areas and comprising a plurality of separated portions;

an insulating layer formed on and covering both said first substrate and said black matrix;

a gate line assembly formed on said insulating layer, said gate line assembly comprising gate lines proceeding in a horizontal direction, and gate electrodes connected to the gate lines;

a gate insulating pattern formed on and covering both said insulating layer and said gate line assembly;

a semiconductor pattern formed on said gate insulating pattern;

an ohmic contact layer formed on said semiconductor pattern;

a data line assembly formed on said ohmic contact layer, said data line assembly comprising a source electrode and a drain electrode separated from each other, and data lines connected to the source electrode while crossing over the gate lines to define the pixel areas; and

a protective layer covering said data line assembly and said gate line assembly while exposing said gate insulating pattern, said semiconductor pattern, and portions of said insulating layer placed at the pixel areas; and

buffer layers placed at the same plane as said gate line assembly or said data line assembly, each buffer layer covering a gap between the separated portions neighboring each other.

5-6. (Cancelled)

7-13. (Withdrawn)

14. (Currently Amended) ~~The~~ A liquid crystal display ~~of claim 2, further~~ comprising:

a first insulating substrate;

a black matrix formed on said first substrate, said black matrix being mesh-shaped with opening portions at pixel areas;

an insulating layer formed on and covering both said first substrate and said black matrix;

a gate line assembly formed on said insulating layer, said gate line assembly comprising gate lines proceeding in a horizontal direction, and gate electrodes connected to the gate lines;

a gate insulating pattern formed on and covering both said insulating layer and said gate line assembly;

a semiconductor pattern formed on said gate insulating pattern;

an ohmic contact layer formed on said semiconductor pattern;

a data line assembly formed on said ohmic contact layer, said data line assembly comprising a source electrode and a drain electrode separated from each other, and data lines connected to the source electrode while crossing over the gate lines to define the pixel areas;

a protective layer covering said data line assembly and said gate line assembly while exposing said gate insulating pattern, said semiconductor pattern, and portions of said insulating layer placed at the pixel areas

a second insulating substrate facing said first insulating substrate; and

a common electrode formed on said second insulating substrate, the common electrode having opening portions over said semiconductor pattern between the neighboring data lines.

15-17. (Cancelled)

18. (Currently Amended) The method ~~of claim 17,~~ for fabricating a thin film transistor substrate for a liquid crystal display, comprising steps of:

forming a black matrix on an insulating substrate, wherein the black matrix is mesh-shaped and has opening portions at pixel areas and comprising a plurality of separated portions;

forming an insulating layer on the substrate such that the insulating layer covers the black matrix;

forming a gate line assembly on the insulating layer, the gate line assembly comprising gate lines proceeding in a horizontal direction, and gate electrodes connected to the gate lines, wherein said gate lines are narrower than the black matrix;

depositing a gate insulating layer onto the insulating layer;

depositing a semiconductor layer onto the gate insulating layer;

forming an ohmic contact layer on the semiconductor layer;

forming a data line assembly on the ohmic contact layer, the data line assembly comprising a source electrode and a drain electrode separated from each other, and data lines connected to the source electrode while crossing over the gate lines to define the pixel areas, wherein said data lines are narrower than the black matrix;

depositing a protective layer onto the substrate such that the protective layer covers the data line assembly and the gate line assembly; and

forming opening portions exposing the insulating layer at the pixel areas by patterning the protective layer, the gate insulating layer and the semiconductor layer,

wherein buffer layers are formed between the separate portions of the black matrix at the step of forming the gate line assembly or the data line assembly.

19. (Cancelled)

20-25. (Withdrawn)